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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GEORGE, PATRICIA ANN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,723	MERRY ET AL.	
	Examiner	Art Unit	
	Patricia A. George	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/31/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections, Specification, Claim Rejections - 35 USC § 112

The amendments filed 9/01/2006 overcome the following objections and rejections of the office action filed 6/15/06: claim 19, amended to typo overcome objections; claim 50 has been amended to resolve the objection to the specification failing to provide proper antecedent basis; and claims 21-27 and 41 have been amended to overcome the 35 U.S.C. 112, second paragraph rejections of indefinite terms.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 19-22, 24-26 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (5,478,766) in view of Ning et al. (6,440,753) and Van Zant (A Practicle Guide to Semiconductor Processing; Semiconductor Services; 1986.

In figure 5E (described in columns 5 and 6) Park et al. discloses a method for processing a film stack, formed on a substrate (21), a first silicon layer (33) underlying the first metal layer (32), a second silicon layer underlying the first silicon layer (layer under 33), and a second metal layer (22) disposed between the second silicon layer and the substrate. Park et al. teaches the first and second silicon layers are etched by using the metal layer as a mask (see col. 6, lines 1-3), which illustrates portions of the first metal layer are etched to become exposed and expose a portion of the first silicon layer, and then to etch the first silicon layer (see figure 5E).

Park is silent as to the etching occur in a process chamber, however it would have been obvious to one of ordinary skill in the art at the time of invention was made, to accomplish the etching steps of Park in any conventional available apparatus, including a process chamber, because Van Zant illustrates (see fig. 13.6) that processing chamber are conventional for etching process. Further, Van Zant teaches that by placing wafers in a chamber (i.e. process chamber) for plasma etching, several problems resulting in wet etching are overcome, such as accurate pattern definition, control of critical dimentions, and undercutting (see section 13.6, which explains the previously referenced figures). Applicants have not shown anything unexpected by employing a conventional piece of apparatus to accomplish the claimed etching steps.

Park et al. is silent as to how the first metal layer (a metal mask) is patterned i.e. the use of photoresist over the metal layer, as the limitation of applicants' claim 1.

Ning et al. illustrates it is commonly known that photoresist is formed on top of a metal layer, used to pattern the metal mask layer (i.e. exposing the metal through the resist), and finally subjected to an ash process where the photoresist is removed.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include photoresist over a metal layer, as Ning et al., when forming the film stack of park et al. because Ning illustrates the photoresist is useful in forming a pattern in the metal layer which is subsequently used as a mask layer, and that it is commonly known and conventional to practice the forming of photoresist over a metal layer.

As to claim 20, Park et al. illustrates a portion of the second silicon layer exposed by the etching of the first silicon layer (see fig. 5E).

As for claims 21 and 22, see discussion toward claim 19, above.

As for claim 25, see the discussion directed toward claim 1 above.

As for claim 26, wherein the step of etching the channel further comprises: leaving a strip of the second silicon layer between the channel and the second metal layer, see Park et al.'s figure 5E.

As for claim 45, Park et al. is silent as to the negative limitation etching without removing the substrate from the processing chamber.

However, it would have been obvious to one of ordinary skill in the art at the time of invention was made, to leave the substrate in the process chamber while etching, as

in Park. et al., because the combined method of Park et al. provides no reason to remove the substrate from the chamber.

Although the combined teaching of Park et al. does not explicitly teach the metal layer exposed through the photoresist to expose a second portion of the first silicon layer, as applicants' limitation of claim 24.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, that several portions of the first silicon layer would have been exposed, as applicant's claimed limitation, as it is intrinsic to etching to expose portions of material being etched.

It also would have obvious to one of ordinary skill in the art at the time of invention was made, that the metal layer exposed through the photoresist to expose a second portion of the first silicon layer, as applicants limitation of claim 24, because etching would intrinsically expose multiple portions of the first silicon layer.

As for claim 46, see discussion above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al., Ning et al., and Van Zant, as applied to claims 19-22, 24-26 and 45-46 above,

further in view of Wolf (Silicon Processing for the VLSI Era; Vol. 1; 1986 lattice Press; pg. 432).

As for claim 23, Park illustrates removing photoresist, however, Park is silent as to thinner sections of photoresist disposed between thicker sections of photoresist.

Wolf teaches it is common for a photoresist layer to have uniformity, i.e. thinner sections of photoresist disposed between thicker sections of photoresist (see page 432, line 5 of Wolf).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include that photoresist has thinner sections of photoresist disposed between thicker sections, as Wolf's uniformity, when exposing and removing the resist, as Park, because Wolf teaches uniformity in the resist layer is a known and monitored as an effect of the resist coating process. Further, Wolf teaches film uniformity is intrinsically a limitation of the spin process that results in pluses and minus.

Claim Rejections - 35 USC § 103

Claims 27 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. and Ning et al. and and Van Zant, as applied to claims 19-23, 25-26 and 45-46 above, further in view of Kabansky (20020179248).

Park et al. is silent as to the step of ashing performed in the processing chamber, as applicants' limitation of claim 27, or without removing from the cluster tool as in claim 47.

Kabansky teaches a method for etching, ashing, or cleaning in the same process chamber (see para. 11), which reads on the limitations of both claims 27 and 47.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the method of processing a stacked film, as Park et al., to include the step of ashing performed in the processing chamber, as Kabansky, because Kabansky teaches as a result, the useful lifetime of the hardware is increased, the generation of unwanted particles from the hardware is reduced, the mean time between maintenance is increased, the stability and integrity of the performance of the etch or clean process is increased, and the overall cost of the process is decreased (see Field of Invention).

Claim Rejections - 35 USC § 103

Claims 28-30, 32-34, and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al., Ning et al., and Van Zant, as applied to claims 19-23, 25-26 and 45-46 above, further in view of Nallan (20020132488).

Park et al. is silent toward specific etch process parameters of metal and silicon etches as applicants' limitation of claims 28-30, 32-34, and 51.

Nallan teaches use of a closed remote plasma cluster tool (see para 23) for etching metal (para 21) and silicon (para0030) by generating the plasma using a plasma source gas in the upper chamber (part 104 of figure 1) and providing a secondary gas (see abstract) as an etchant (i.e. to the process chamber), as in claim 28 and 32.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the specifics of the etching process, as Nallan, when processing a stacked film, as Park, because Nallan teaches etching process which is a particularily useful improvement which controls the profile and etching rates (para 0016).

As to claims 29-30 and 33-34, Nallan teaches it is useful to use a high density plasma with a RF bias power applied to the semiconductor substrate (see abstract and para. 0025).

As to claim 51, see discussion above.

Claim Rejections - 35 USC § 103

Claims 31 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. Ning et al., and Van Zant, as applied to claims 19-26 and 45-46 above, further in view of Kropewnicki (6440864).

Park et al. fail to disclose the second process gas is chlorine or O2, as in the limitations presented by applicants in claims 31, and 35-36.

Kropewnicki teaches the process gasses applicants claim (such as chlorines and oxygen) and that they may be introduced in sequential orders (i.e. second process gas) to provide high etching rates, and high selectivity (see col.3, line 12-35).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include that second process gas is chlorine or O2, as in the limitations presented by applicants in claims 31, and 35-36, when processing the

stacked film, as Park, because Kropewnicki teaches gasses may be introduced in specific orders to provide high etching rates, and high selectivity).

Claim Rejections - 35 USC § 103

Claims 37-44, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al., Ning et al., and Van Zant, as applied to claims 19-26 and 45-46 above, further in view of Kropewnicki (6440864), Perlov(6283692), and Chien et al. (20020192957).

Park et al. is silent as to the steps of ashing the resist, post ash residue removal, and passivation of the same area, as well as the modular process parameters as in applicants claims 37-42.

Kropewnicki teaches removing resist (i.e. ashing) (see col. 6, line 60) and etch residues (see col. 6, line 61); through use of an Centura (i.e cluster tool) ((see col. 11, line 54), as the limitation of applicants' claims 37 and 38; deposing a passivation layer after residue removal in a chamber (i.e. deposition occurs thus the chamber is a deposition chamber) in the processing chamber where the etch occurred, (i.e. in same cluster tool) as in claims 39 –41 (see col. 13, lines 37-60); ashing and etching may occur in the same processing chamber (see col. 6, line 30-47), as in applicants' claim 42; and transferring the substrate to a residual removal station (see col. 6, line 30-47), as in claim 43.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the steps of ashing the resist, post ash residue removal,

and passivation of the same area, as well as the modular process parameters as in applicants claims 37-42, when forming the stacked layer, as Park, because Kropewnicki teaches these steps are known and effective for patterning a stacked layer.

Park et al is silent as to the limitation of process stations being coupled to a factory interface, as in claim 43 and 44.

Perlov teaches a method for storing cassettes and transferring them between processing stations (i.e. process stations being coupled to a factory interface), as in applicants' claims 43-44 (see summary of invention).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to couple a factory interface to the process stations, as Perlov, when processing the film stack of park, because Perlov teaches system down time is reduced or eliminated (see background), an well known cost savings to manufacturing.

Park does not teach the passivation layer, of applicants' claim 39, is deposited after the residue removal step.

Chien et al. teaches it is known to passivate after etching (i.e. etching, ashing and residue removal). Chien et al. illustrates a process for residue removal then passivation (see para. 22-23), as applicants' limitation of claim39.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the step of pasivation after removing etch residues, as Chien et al., when processing the stacked layers, as Park, because Chien teaches a

known process which enhances the quality of the chip and saves production costs, also shortens the production period, thus increasing productivity. (see para. 23)

Claim Rejections - 35 USC § 103

Claims 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over the modified teaching of Park et al., Ning et al., Van Zant, Kropewnicki, Perlov, and Chien et al., as applied to claims 37-44, and 48 above, further in view of Minnick et al. (6260894).

Park failed to teach depositing a dielectric on a substrate without removing the substrate from the cluster tool.

Minnick teaches processing may undergo any one of a several possible processes, such as oxidation, nitridation, anneal, deposition, or etch, in the same cluster tool (see col.3, lines 1-12).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the invention of forming stacked layers by using the same cluster tool, as Park, for any number of process such as etch and deposition, as Minnick, because Minnick illustrates it is an effective method of manufacturing which has the added benefit of cost savings.

Claim Rejections - 35 USC § 103

Claims 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over the modified teaching of Park et al., as applied to claims 28-30, 32-34, 51, and 53

above, further in view of Wolf et al (Vol. 1, Process Technology, 1986, Lattice Press, figure 5, page 546-547).

Park is silent as to the rf power used to energize the plasma, as in claim 52.

Wolf teaches excitation power (i.e. rf power) is a process parameter (see page 546) controlled through routine experimentation (see page 547).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include that the process parameter of rf power can be modified throught routine experimentation to achieve desired results, as in Wolf, when processing a film stack, as in Park et al., because Wolf teaches it is useful to control such parameters (see page 547).

As to claim 53, see discussion above.

Response to Arguments

Applicant's arguments filed 9/01/2006 have been fully considered but they are not persuasive.

In response to applicant's repeated argument, on pages 12-14 that Park addresses a totally different problem from applicants, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

In response to applicants' argument, on page12 and 13, that there is no motivation to combine Park's teaching with those of Van Zant or Ning motivation is proper because:

One skilled in the semiconductor art, would clearly be motivated to etch in a process chamber, because van Zant illustrates (see fig. 13.6) that using process chambers are conventional for etching process. Further, van Zant teaches that by placing wafers in a chamber (i.e. process chamber) for plasma etching, several problems resulting in wet etching are overcome, such as accurate pattern definition, control of critical dimentions, and undercutting (see section 13.6, which explains the previously referenced figures).

One skilled in the semiconductor art, would be fully motivated to implore use of photoresist over a metal layer to pattern and expose the layer, because Ning et al. illustrates it is commonly known that photoresist is formed on top of a metal layer to pattern the metal mask layer (i.e. exposing the metal through the resist), and finally subjected to an ash process where the photoresist is removed. Further, it would have been obvious to one of ordinary skill in the art at the time of invention was made, to include photoresist over a metal layer, as Ning et al., when forming the film stack of park et al. because Ning illustrates the photoresist is useful in forming a pattern in the metal layer which is subsequently used as a mask layer, and that it is commonly known and conventional to practice the forming of photoresist over a metal layer.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571)272-5955. The examiner can normally be reached on weekdays between 7:00am and 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571)272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PAG
10/06

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